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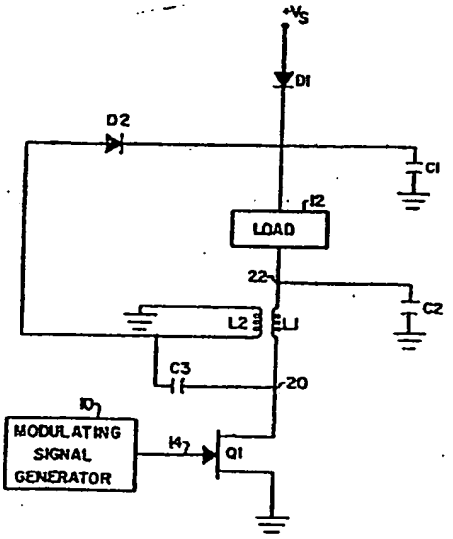
(54) Title: EFFICIENT CURRENT MODULATOR USEFUL WITH INDUCTIVE LOADS

(57) Abstract

A current modulator for modulating the current flowing through a load (12) from a DC power supply (V_s) to circuit ground. A switching device (Q1) is connected between the load (12) and circuit ground for varying the current through the load (12) in response to a modulating signal (14) applied to the switching device (Q1). A first inductance coil (L1) is connected between the switching device (Q1) and the load (12). A second inductance coil (L2) is mutally coupled to the first coil (L1) for receiving energy induced in the first coil (L1) by the current variations. The second coil (L2) is conductively isolated from the first coil (L1). A diode (D2) is connected between the second coil (L2) and the power supply side of the load (12) for transferring the received energy back to the power supply side of the load (12).



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"EFFICIENT CURRENT MODULATOR USEFUL WITH INDUCTIVE LOADS"

BACKGROUND OF THE INVENTION

The present invention pertains to current modulators and is particularly directed to enhancing the utility and improving the efficieny of current modulators that are used for modulating the current flowing through a load from a DC power supply to circuit ground.

In prior art current modulators of this type, a switching device is connected between the load and circuit ground for varying the current through the load in response to a modulating signal applied to the switching device. An overshoot clipping diode is connected between the switching device and the power supply side of the load for protecting the load and the switching device and the power supply side of the load for protecting the load and the switching device from excessively high currents.

Such prior art current modulator cannot be operated to produce an alternating current through an inductive load. Because the voltage at the switching device side of the load would exceed the power supply voltage during each half cycle, whereby the diode would become forward biased and effectively cause a short circuit across the load.

SUMMARY OF THE INVENTION

The present invention provides an efficient current modulator that is useful with inductive loads.

The present invention is a current modulator for modulating the current flowing through a load from a DC power supply to circuit ground, including a switching device connected between the load and circuit ground for varying the current through the load in response to a modulating signal applied to the switching device; a first inductance coil connected between the switching device and the load; a second inductance coil mutually coupled to the first coil for receiving energy induced in the first coil by the current variations; and a diode coupled between the second coil and the power supply side of the load for transferring the received energy to the power supply side of the load. The second inductance coil is conductively isolated from the first inductance coil. As a result when the diode becomes forward biased for transferring energy to the power supply side of the load, it nevertheless does not cause a short circuit across an inductive load.

Because energy is returned to the power supply side of the load by the diode, the current modulator of the present invention is more efficient.

The efficiency of the current modulator is further increased by using a high frequency switching device. Less power is lost in a high frequency switching device because it has shorter turn-on time.

The efficiency of the current modulator is still further enchanced by providing that the mutually coupled inductance coils have an air core. The combination of air core inductance coils and switching at a high frequency reduces heat loss in the inductance coils.

Additional features of the present invention are described in the description of the preferred embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a combination block and schematic circuit diagram of a preferred embodiment of the current modulator of the present invention.

Figure 2 is a schematic circuit diagram of the modulating signal generator included in the current modulator of Figure 1.

Figures 3A through 3E illustrate waveforms of signals produced in the modulating signal generator of Figure 2.

Figure 4 is a combination block and schematic circuit diagram of another preferred embodiment of the current modulator of the present invention.

Figure 5 is a schemtatic circuit diagram of the modulating signal generator included in the current modulator of Figure 4.

Figures 6A through 6F illustrate waveforms of signals produced in the modulating signal generator of Figure 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, a preferred embodiment of the current modulator of the present invention includes a high frequency switching device Q1, a first inductance coil L1, a second inductance coil L2, two diodes D1 and D2, three capacitances C1, C2 and C3 and a modulating signal generator 10. The switching device Q1 is a VMOS FET power transistor which is capable of switching at high frequencies. The transistor Q1 is connected between a load 12 and circuit ground for varying the current through the load 12 in response to a modulating signal applied on line 14 to the gate of the transistor Q1 from the modulating signal generator 10. A DC power supply terminal V_S is coupled to the other side of the load 12 by a protective diode D1. The load 12 is isolated from circuit ground by the capacitances C1 and C2.

The first inductance coil L1 is connected between the transistor Q1 and the load 12. The second inductance coil L2 is mutually coupled to the first inductance coil L1 for receiving energy that is induced in the first inductance coil L1 by variations in the current through the load 12. The first and second inductances L1, L2 are tightly wound on an air-filled core by a bifilar, or preferably a coaxial winding.

The first and second inductances L1, L2 are conductively isolated from each other, i.e. there is no DC current path between the coils L1 and L2. However, the coils L1 and L2 are coupled by the capacitance C3 to minimize any problems that could arise due to poor mutual coupling between the coils L1 and L2.

The diode D2 is connected between the second inductance coil L2 and the power supply side of the load 12 for transferring the received energy from the second coil L2 to the power supply side of the load 12.

The modulating signal generator 10 is adopted for applying a high frequency pulsed modulating signal to the gate of the switching transistor Q1. The high frequency chosen in this preferred embodiment is 100 kHz.

A preferred embodiment of the modulating signal generator 10, as shown in Figure 2, includes a free running oscillator consisting of a Schmitt inverter I1, a resistance R1 and a capacitance C4 for providing a high frequency pulsed square wave signal on line 16, as illustrated in Figure 3A. The resistance R1 is connected between the input and output of the inverter I1 and the capacitance C4 is connected between the input of the inverter I1 and circuit ground.

The modulating signal generator 10 further includes a differentiating circuit consisting of a capacitance C5 and a resistance R2; an npn transistor Q2; a current limiting resistance R3; a capacitance C6 and a comparator consisting of a high gain amplifier A1.

The square wave signal on line 16 is differentiated by the differentiator circuit C5, R2 to cause the transistor Q2 to be turned on each time there is a positive going transition in the square wave on line 16. The capacitance C6 is discharged each time the transistor Q2 is turned on, but then is charged by the current through the resistance R3 from a DC supply voltage terminal V_C while the transistor Q2 is turned off. As a result, a sawtooth waveform is provided on line 18 to one input terminal of the comparator A1, as shown by the solid line in Figures 3B and 3D.

A low frequency reference signal V_R is applied to the other input terminal of the comparator A1 for comparison with the sawtooth signal on line 18. The frequency of the reference signal V_R is chosen in accordance with what predetermined low frequency the current through the load 12 is to be varied. Typically, the predetermined low frequency is 50 or 60 Hz.

The amplitude of the reference signal V_R varies at the predetermined low frequency. When the reference signal V_R has a relatively high amplitude (as shown in Figure 3B), a pulsed high frequency modulating signal having a relatively short duty cycle (as shown in Figure 3C) is provided on line 14 from the output of the comparator A1 to the gate of the switching transistor Q1 (Figure 1). When the reference signal has a relatively low amplitude (as shown in Figure 3D), a pulsed high frequency modulating signal having a relatively long duty cycle (as shown in Figure 3E) is provided on line 14 from the output of the comparator A1.

The amplitude of the current through the load 12 is proportional to the amount of time that the switching transistor Q1 is turned on, which is in turn proportional to the duty cycle of the pulsed high frequency modulating signal. Accordingly, the current through the load 12 is varied at the predetermined low frequency of the reference signal V_R.

The inductance value of the first inductance coil L1 is chosen to have enough inductance to allow only negligible current to build up when the pulsed modulating signal on line 14 has a minimum discrete duty cycle, and to allow a relatively large current to build up when the pulsed modulating signal on line 14 has a maximum discrete duty cycle. When the current through the first inductance coil L1 is terminated during each pulse upon the switching transistor Q1 being turned off, the stored energy in the two mutually coupled inductance coils L1 and L2 results in a high positive voltage at point 20 on the switching transistor side of the first coil L1. This is commonly known as overshoot. Overshoot is minimized in the current modulator of the present invention by coupling induced energy from the first coil L1 to the second coil L2 and returning the energy received by the second coil L2 back to the power supply side of the load 12 via the diode D2. If overshoot was not minimized, it typically would damage the switching transistor Q1 and the first coil L1. The energy that returned back to the power supply side of the load 12 via the diode D2 reduces the current that must be supplied from the power supply terminal V_S through the diode D1 by an amount equal to the average current through the diode D2.

In the current modulator of Figure 1, when the instantaneous voltage at point 22 on the switching transistor side of the load 12 exceeds the power supply voltage V_S, the diode D2 does not short circuit the load 12 because the inductance coils L1 and L2 are not conductively coupled to each other, whereby there is no DC current path from the point 22 through the diode D2 back to the power supply side of the load 12. As a result, the instantaneous voltage at the point 22 may swing to as much as twice the power supply voltage V_S.

As the switching transistor Q1 is switched on with a short turn-on time, there will be minimum loss in the transistor Q1 during the turn-on time because there is low current in the inductance L1 for a fast step change. If the saturation voltage

on the transistor Q1 is low, the average power lost in the transistor Q1 may be minimized during its "on" time and if the transistor Q1 is turned off with a very short turn-off time, the losses across the transistor Q1 during turn-off may be kept quite small. Therefore, switching at a high frequency is preferred.

The coils L1 and L2 have a very low resistance, whereby the heat losses in these coils L1 and L2 are quite small. Typically, the current modulator of Figure 1 will deliver 96 percent of input power into the load with four percent being dissipated in the combination of the coils L1 and L2, the switching transistor Q1 and the diode D2.

A preferred embodiment of the current modulator of the present invention that is particularly adapted for use with a transformer as a load is described with reference to Figures 4, 5 and 6. The load is the primary winding S of the transformer T1 is connected between an output terminal V_0 and circuit ground.

The current modulator includes first and second high frequency switching devices Q11 and Q12. As in the preferred embodiment of Figure 1, the switching devices Q11 and Q12 are VMOS FET power transistors which are capable of switching at high frequencies, such as 100 kHz.

The current modulator of Figure 4 further includes first, second, third and fourth inductance coils L11, L12, L13 and L14, first and second diodes D11 and D12, capacitances C11 and C12 and a modulating signal generator 24.

The primary winding P has a center tap 26 that is connected to a DC power supply terminal V_S.

The first switching transistor Q11 is connected between one side 28 of the primary winding P and circuit ground for varying the current through the primary winding P in response to the first modulating signal applied on line 30 to the gate of the switching transistor Q11 from the modulating signal generator 24.

The first inductance coil L11 is connected between the first transistor Q11 and the one side 28 of the primary winding P.

The second inductance coil L12 is mutually coupled to the first inductance coil L11 for receiving energy induced in the first coil L11 by the current variations. The first and second coils L11, L12 are tightly wound on an air-filled core by a bifilar or preferably a coaxial winding. The first and second coils L11, L12 are conductively isolated from each other.

The first diode D11 is coupled between the second coil L12 and the other side 32 of the primary winding P for transferring the received energy from the second coil L12 through the other side 32 of the primary winding P to the power supply terminal V_S.

The second switching transistor Q12 is connected between the other side 32 of the primary winding P and circuit ground for varying the current through the primary winding P in response to a second modulating signal applied on line 34 to the gate of the second switching transistor Q12 from the modulating signal generator 24.

The third inductance coil L13 is connected between the second transistor Q12 and the other side 32 of the primary winding P.

The fourth inductance coil L14 is mutually coupled to the third inductance coil L13 by the current variations. The third and fourth coils L13, L14 are rightly wound on an air filled core by a bifilar or preferably a coaxial winding. The third and fourth coil are conductively isolated from each other.

The second diode D12 is coupled between the fourth coil L12 and the one side 28 of the primary winding P for transferring the received energy from the fourth coil L14 through the one side 28 of the primary winding P to the power supply terminal V_S.

The modulating signal generator 24 is adapted for applying the first and second modulating signals to the respective gates of the switching transistors Q11 and Q12. The first and second modulating signals are applied in such a manner as to cause only one side of the primary winding P to be connected to circuit ground at any one time.

A preferred embodiment of the modulating signal generator 24, as shown in Figure 5, includes an oscillator circuit consisting of a first hysteresis inverter G1, a resistance R11 connected between the input and the output of the inverter G1 and a capacitance C11 connected between the input of the inverter G1 and circuit ground.

The modulating signal generator 24 further includes a second hysteresis inverter G2 having its input connected to the output of the inverter G1; an input amplifier A2, and resistances R12, R13, R14 and R15. A reference signal terminal V_R is connected through the resistance R12 to the inverting input terminal of the amplifier A2. The inverting input terminal is also connected through the resistance R13 to a power supply terminal V_C. The non-inverting input terminal of the amplifier A2 is connected to circuit ground. The resistance R14 is connected between the inverting input and the output of the amplifier A2. The output of the amplifier A2 is connected through the resistance R15 to the input of the first hysteresis inverter G1.

The oscillator circuit G1, R11, C11 provides a square wave pulsed signal on line 30, as shown in Figure 6A. The inverter G2 inverts the signal on line 30 to provide a complementary square wave pulsed signal on line 34. If the signals on lines 30 and 34 each have the same duty cycle, the average current through the primary winding P of the transformer T1 in the current modulator of Figure 4 will be zero.

When the output of the inverter G1 on line 30 switches high, the capacitance C11 is charged through the resistance R11 to provide a signal at the input terminal 36 of the inverter G1 having a waveform as shown in Figure 6B. When the voltage of the signal at input terminal 36 rises to the upper switching threshold V_2 of the inverter G1, the output of the inverter G1 switches low as shown in Figure 6A. The capacitance C11 is then discharged through the resistance R11 until the voltage of the signal at the input terminal 36 drops to the lower switching threshold V_1 of the inverter G1, at which point, the inverter G1 again switches high.

The duty cycle of the pulsed signal provided on lines 30 and 34 from the respective outputs of the inverters G1 and G2 is varied by varying the rate at which the capacitance C11 is charged or discharged. This is accomplished by varying the current through the resistance R15 to the input terminal 36 of the inverter G1. Such current variation is caused in response to a reference signal having a predetermined low frequency that is applied to the reference signal terminal V_R. The frequency of reference signal is chosen in accordance with what predetermined low frequency the current through the primary winding P of the transformer T1 is to be varied. Typically, the predetermined low frequency is 50 or 60 Hz.

The amplifier A2 inverts the reference signal applied to the terminal V_R and causes a current to be provided through the resistance to R15 the inverter input terminal 36 that either aids or opposes the current through the resistance R11 in charging or discharging the capacitance C11.

When the voltage at the output terminal 38 of the amplifier A2 is negative with respect to the average value of the voltage at the inverter input terminal 36, the capacitance C11 is charged slowly and discharged quickly, as shown in Figure 6C. This causes the first inverter output signal on line 30 to have a long duty cycle, as shown in Figure 6D. Conversely, the pulsed output signal of the second inverter G2 simultaneously has a short duty cycle.

When the voltage at the output terminal 38 of the amplifier A2 is positive with respect to the average value of the voltage at the inverter input terminal 36, the capacitance C11 is charged quickly and discharged slowly, as shown in Figure 6E. This causes the first inverter output signal on line 30 to have a short duty cycle as shown in Figure 6F. Conversely, the pulsed output signal of the second inverter G2 simultaneously has a long duty cycle.

The imbalance in the duty cycles of the pulsed modulating signals applied to the respective gates of the switching transistors Q11 and Q12 causes the average current flow through the primary winding P of the transformer T1 to be other than zero. The amount of current flow through the primary winding P is proportional to the difference between the duty cycles of the pulsed modulating signals applied on lines 30 and 36 to the respective gates of the switching transistors Q1 and Q2.

Current flow through the primary winding P is greater in the direction from the center tap 26 toward the one side 28 when the duty cycle of the pulsed modulating signal on line 30 is greater than the duty cycle of the pulsed modulating signal on line 34.

The variation in the amplitude and direction of current flow through the primary winding P is in response to the variation of instantaneous voltage at the amplifer output terminal 38 in the modulating signal generator 24. Thus by providing a predetermined low frequency reference signal to the reference signal terminal V_R, an output signal having the prefetermined low frequency is produced at the output terminal V_0 of the secondary winding of the transformer T1. Accordingly, the current modulator of Figure 4 is particularly useful for providing a low distortion sine wave low frequency output signal.

When the voltage at the output terminal 38 of the amplifier A2 is positive with respect to the average value of the voltage at the inverter input terminal 36, the capacitance C11 is charged quickly and discharged slowly, as shown in Figure 6E. This causes the first inverter output signal on line 30 to have a short duty cycle as shown in Figure 6F. Conversely, the pulsed output signal of the second inverter G2 simultaneously has a long duty cycle.

The imbalance in the duty cycles of the pulsed modulating signals applied to the respective gates of the switching transistors Q11 and Q12 causes the average current flow through the primary winding P of the transformer T1 to be other than zero. The amount of current flow through the primary winding P is proportional to the difference between the duty cycles of the pulsed modulating signals applied on lines 30 and 36 to the respective gates of the switching transistors Q1 and Q2.

Current flow through the primary winding P is greater in the direction from the center tap 26 toward the one side 28 when the duty cycle of the pulsed modulating signal on line 30 is greater than the duty cycle of the pulsed modulating signal on line 34.

The variation in the amplitude and direction of current flow through the primary winding P is in response to the variation of instantaneous voltage at the amplifer output terminal 38 in the modulating signal generator 24. Thus by providing a predetermined low frequency reference signal to the reference signal terminal V_R, an output signal having the prefetermined low frequency is produced at the output terminal V_0 of the secondary winding of the transformer T1. Accordingly, the current modulator of Figure 4 is particularly useful for providing a low distortion sine wave low frequency output signal.

Basically, the operation and specifics of construction of the respective combinations of the switching transistor Q11, the inductance coils L11, L12 and the diode D11 and the switching transistor Q12, the inductance coils L13, L14 and the diode D12 in the current modulator of Figure 4 are the same as those of the combination of the switching transistor A1, the inductance coils Q1, Q2 and the diode D1 in the current modulator of Figure 1.

A unique feature of the current modulator of Figure 4 is the use of the energy recovery path through the primary winding P to provide additional efficiency. This may be seen as follows: If the two diodes, D11 and D12 had their cathodes connected to the power supply terminal V_S. The received energy from the coil L2 and L4 still would be returned to the power supply. However, when these two diodes D11 and D12 are cross-connected to the opposite sides 28, 32 of the primary winding P, as shown in Figure 4, then the recovered energy flows not only back to the power supply, but returns to the power supply through the opposite non-conducting side of the primary winding, and thereby provides added volt-ampere turns to the transformer T1. Since the recovered energy from the collapsing field of the inductance coils tries to generate a high voltage "inductive kick" that is clipped by diodes D11 and D12, the current through these diodes D11, D12 tends to be relatively constant for different voltages during the energy recovery period.

CLAIMS

1. A current modulator for modulating the current flowing through a load from a DC power wupply to circuit ground, comprising

a switching device connected between the load and circuit ground for varying the current through the load in response to a modulating signal applied to the switching device;

a first inductance coil connected between the switching device and the load;

a second inductance coil mutually coupled to the first coil for receiving energy induced in the first coil by said current variations, the second coil being conductively isolated from the first coil; and

a diode coupled between the second coil and the power supply side of the load for transferring the received energy to the power supply side of the load.

2. A current modulator according to claim 1, wherein the switching device is a high frequency switching device.

3. A current modulator according to claim 2, further comprising

means for applying a high frequency pulsed modulating signal to the switching device.

4. A current modulator according to claim 3, wherein the switching device is a MOS semiconductor device.

5. A current modulator according to claim 4, wherein the switching device is a VMOS FET power transistor.

6. A current modulator according to claims 3 or 5, wherein the means for applying the modulating signal to the switching device comprises

first means for generating a high frequency pulsed signal; and

second means for varying the duty cycle of the pulsed signal at a predetermined low frequency to thereby provide the high frequency pulsed modulating signal for varying the current through the load at the predetermined low frequency.

7. A current modulator according to claim 6, wherein the second means is adapted for varying said duty cycle in response to a reference signal having said predetermined low frequency.

8. A current modulator according to claim 3, wherein the inductance coils have an air core.

9. A current modulator for modulating the current flowing through a load to circuit ground from a DC power supply connected to the load, comprising

a first switching device connected between one side of the load and circuit ground for varying the current through the load in response to a first modulating signal applied to the first switching device;

a first inductance coil connected between the first switching device and the one side of the load;

a second inductance coil mutually coupled to the first coil for receiving energy induced in the first coil by said current variations, the second coil being conductively isolated from the first coil;

a first diode coupled between the second coil and the power supply for transferring the received energy from the second coil to the power supply;

a second switching device connected between the other side of the load and circuit ground for varying the current through the load in response to a second modulating signal applied to the second switching device;

a third inductance coil connected between the second switching device and the other side of the load;

a fourth inductance coil mutually coupled to the third coil for receiving energy induced in the third coil by said current variations, the fourth coil being conductively isolated from the third coil;

a second diode coupled between the fourth coil and the power supply for transferring the received energy from the fourth coil to the power supply; and

means for applying the modulating signals to the switching devices to cause only one side of the load to be connected to ground at any one time.

10. A current regulator according to claim 9,

wherein the first diode is coupled between the second coil and the other side of the load for transferring the received energy from the second coil through the other side of the load to the power supply; and

wherein the second diode is coupled between the fourth coil and the one side of the load for transferring the received energy from the fourth coil through the one side of the load to the power supply.

11. A current regulator according to claim 10, for use with a load having a center tap, further comprising means for connecting the center tap to the power supply.

12. A current regulator according to claim 10, wherein the switching devices are high frequency switching devices.

13. A current modulator according to claim 12, wherein the switching devices are MOS semiconductor devices.

14. A current modulator according to claim 13, wherein the switching device is a VMOS FET power transistor.

15. A current modulator according to claim 12, wherein the means for applying the modulating signals to the switching devices are adapted for applying high frequency pulsed modulating signals.

16. A current modulator according to claims 14 or 15, wherein the means for applying the modulating signals to the switching devices comprises

a first means for generating first and second high frequency pulsed signals that are complementary to each other; and

second means for varying the duty cycles of the first and second high frequency pulsed signals at a predetermined low frequency to thereby provide the first and second modulating signals for varying the current through the load at the predetermined low frequency.

17. A current modulator according to claim 16, wherein the second means is adapted for varying said duty cycles in response to a reference signal having said predetermined low frequency.

18. A current modulator according to claim 15, wherein the inductance coils have air cores.

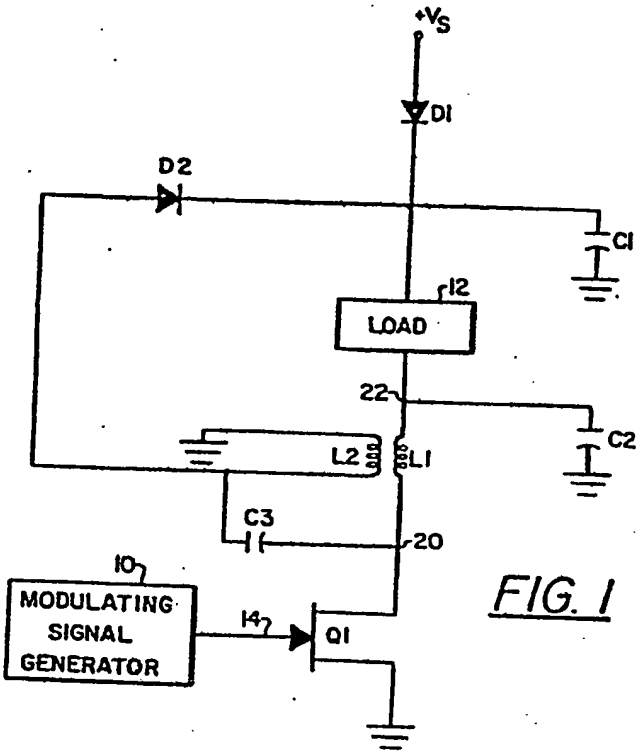

FIG. 1

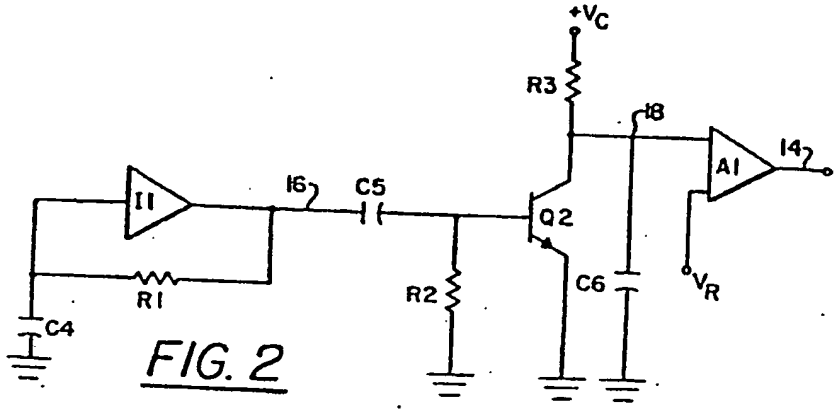

FIG. 2

FIG. 3A

FIG. 3B

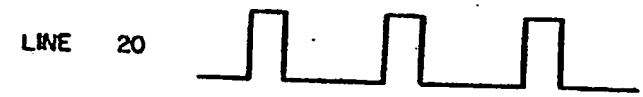

FIG. 3C

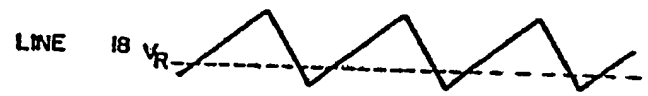

FIG. 3D

FIG. 3E

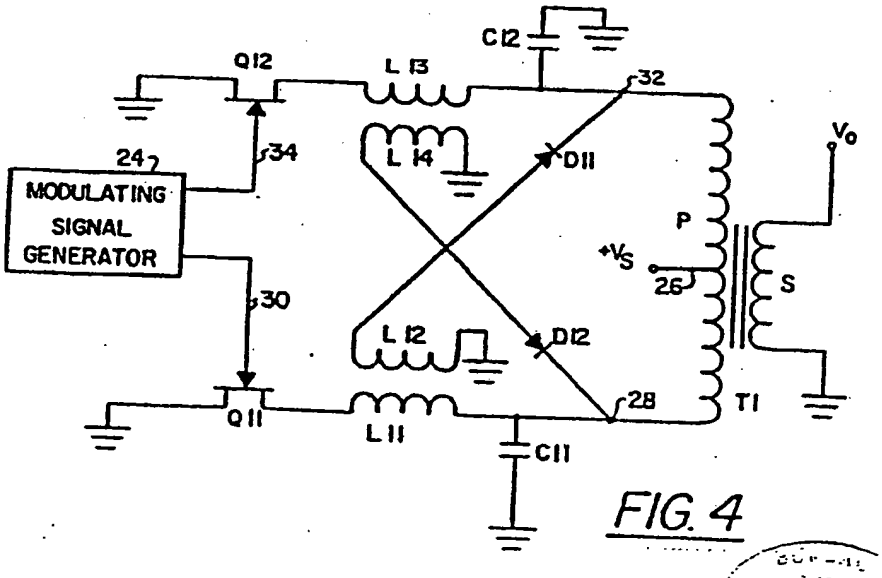

FIG. 4

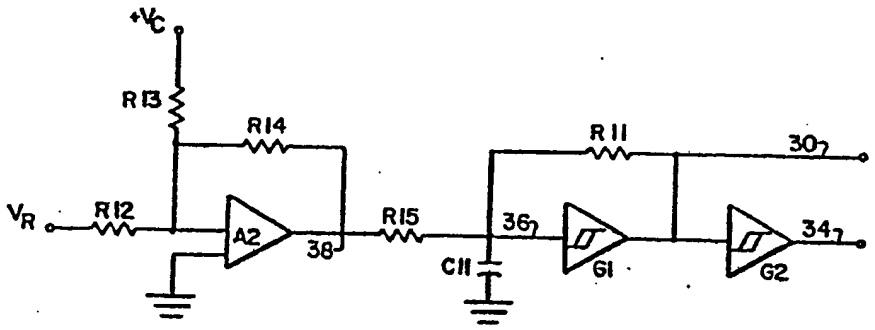

FIG. 5

FIG. 6A

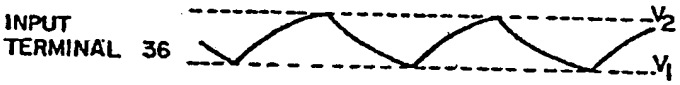

FIG. 6B

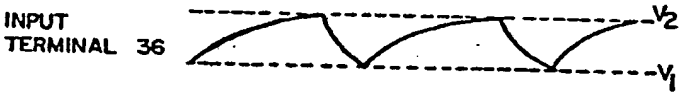

FIG. 6C

FIG. 6D

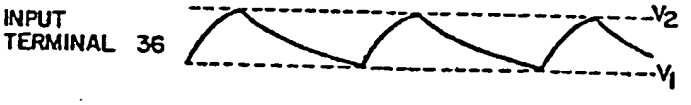

FIG. 6E

FIG. 6F

INTERNATIONAL SEARCH REPORT

International Application No PCT/US82/01243

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) 6

According to International Patent Classification (IPC) or to both National Classification and IPC

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II. FIELDS SEARCHED

Minimum Documentation Searched 4

Classification System	Classification Symbols
U.S.	363/18-26, 97-98, 133-134, 139 323/222, 282-290

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched 5

III. DOCUMENTS CONSIDERED TO BE RELEVANT 14

Category *	Citation of Document, 16 with indication, where appropriate, of the relevant passages 17	Relevant to Claim No. 18
A	US,A, 2,920,259 Published 5 Jan. 1960, Light	
A	US,A, 4,268,898 Published 19 May 1981, Brown	
A	US,A, 4,021,720 Published 3 May 1977, Linnman	
A,P	US,E, 4,336,587 Published 22 Jun 1982, Boettcher, Jr. et al.	
A	EDN, Volume 25, No. 17, Published 20 Sept. 1980, D. Mele, '100-KHZ DC/DC Converter Uses Fets', See Pages 191-192.	

* Special categories of cited documents: 15

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"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search 3	Date of Mailing of this International Search Report 3
15 Nov 1982	23 NOV 1982
International Searching Authority 1	Signature of Authorized Officer 20
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OPTIMIZING CONVERTER DESIGN AND PERFORMANCE UTILIZING MICRO CONTROLLER SYSTEM FEEDBACK AND CONTROL

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Abstract

This paper presents a description of a switching converter design based on a digital philosophy which incorporates proportional and derivative feedback controls to regulate the output voltage. Converter design and performance is optimized by using offset and scaling in the "analog" feedback loop and includes a balance control and "feedforward or anticipatory" pulse width modulation scheme. The novel features, such as system protection and fault isolation diagnostic functions, along with hardware implementation, are discussed and outlined. The performance results of the hardware implementation are also presented at the end of this paper.

1.0 INTRODUCTION

Traditionally, off-line analog switching regulator designs have resulted in a high component count which adversely affects reliability, package size and overall cost. Analog feedback control systems experience both short and long term stability problems because of component drift. Secondly, each output voltage to be regulated requires a dedicated analog control system. This means that power systems which produce multiple, independent, regulated output voltages must have an independent analog controller for each voltage since many contemporary applications require three to five independent voltages, duplicated analog circuitry contributes significantly to the cost of their power systems. Analog designs are not flexible enough to adapt to widely varying applications.

An ideal feedback control system would be one that could incorporate the advantages of proportional and derivative control for multiple, independent, regulated output voltages at low cost in a simple implementation that is relatively independent of component drift and would adapt to different needs. A feedback control system with all these properties can be achieved by using a digital control philosophy instead of an analog one. All the digital functions could be incorporated into a single LSI circuit chip and produce them economically in a small package size. The digital power system controller (DPSC) provides easy manipulation of numerical reference values and control parameters. This makes a single circuit adaptable to widely varying applications providing a great deal of flexibility.

1.1 OBJECTIVES AND FEATURES

The objectives of the DPSC concept are three fold: (1) to provide the pulse width modulation control for the power supply regulation, (2) to provide system protection and, (3) to provide fault isolation (diagnostic) capability in the event of power supply failure.

A switching regulator which uses digital logic as

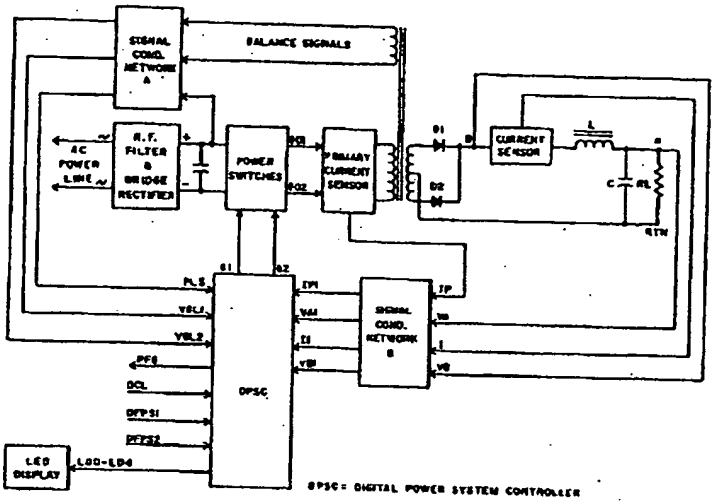


FIGURE 1
COMPLETE DIGITAL POWER SYSTEM

its building blocks to provide proportional/derivative control for minimization of static and dynamic load changes on regulated level and an "anticipatory or feedforward" control for minimization of static and dynamic line changes is outlined. In addition, the digital controller provides the following features:

(1) Frequency programmability up to and beyond 80 kHz to cover bipolar and MOS transistor technologies

(2) Programmable duty cycle limiters for safe operation of a power supply in case of single or double ended rectification schemes.

(3) Drive phase balance control to eliminate the need for a line coupling capacitor in half bridge configurations

(4) Sequencing control of a power system (including power line sense logic)

(5) Remote voltage margin control for field adjustment and evaluating equipment performance

(6) Fault identification diagnostics.

GLOSSARY OF TERMS

$\Phi 1$ and $\Phi 2$: These are two duty ratio drive signals that control the output of the power switches.

PFS: This is the "power fail sense" signal, used to initiate an orderly shut down of the system, being driven by the digital power system.

LD0-LD4: The outputs that provide coded fault isolation data to the LED's for display.

V_{AI}: This is a dc level proportional to the regulated voltage at A.

II: Voltage level proportional to the current at I.

V_{BI}: These are voltage pulses proportional to those at B.

V_{BL1} and V_{BL2}: These are balance signals used to maintain a long term volt-second differential between $\Phi 01$ and $\Phi 02$ approaching 0 in order to limit the transformer magnetizing current.

PLS: This is a "power loss sense" signal. It senses when the bulk voltage rises above or falls below a certain level of its "on" value reference point. When a rising transition is detected,

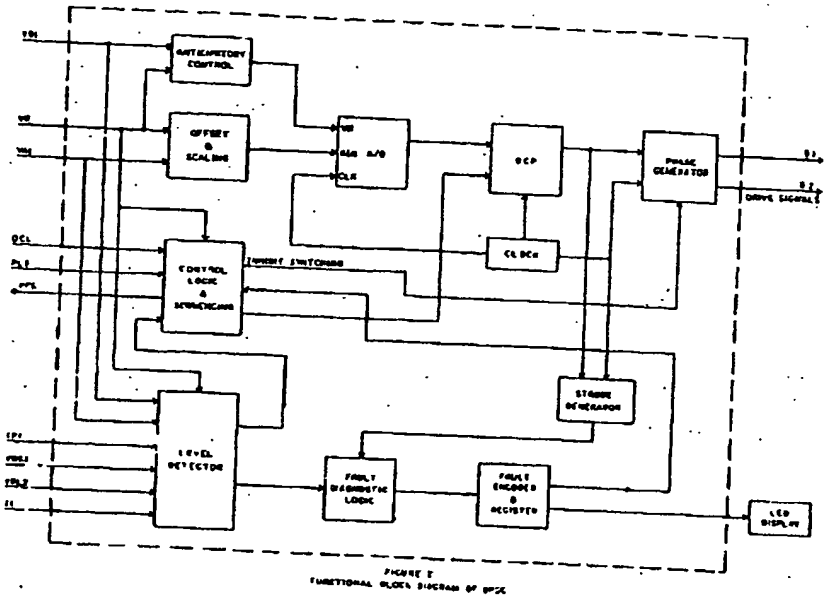


FIGURE 2
FUNCTIONAL BLOCK DIAGRAM OF DPSC

DPSC is initialized and the power up sequence initiated. When a falling transition is detected, PFS signal is activated.

DCL: Programming pin to indicate double ended or single ended rectification scheme.

DFPS1-DFPS2 (Digital Frequency Programmability Signals): Selection of switching frequency will be made according to levels presented on these pins.

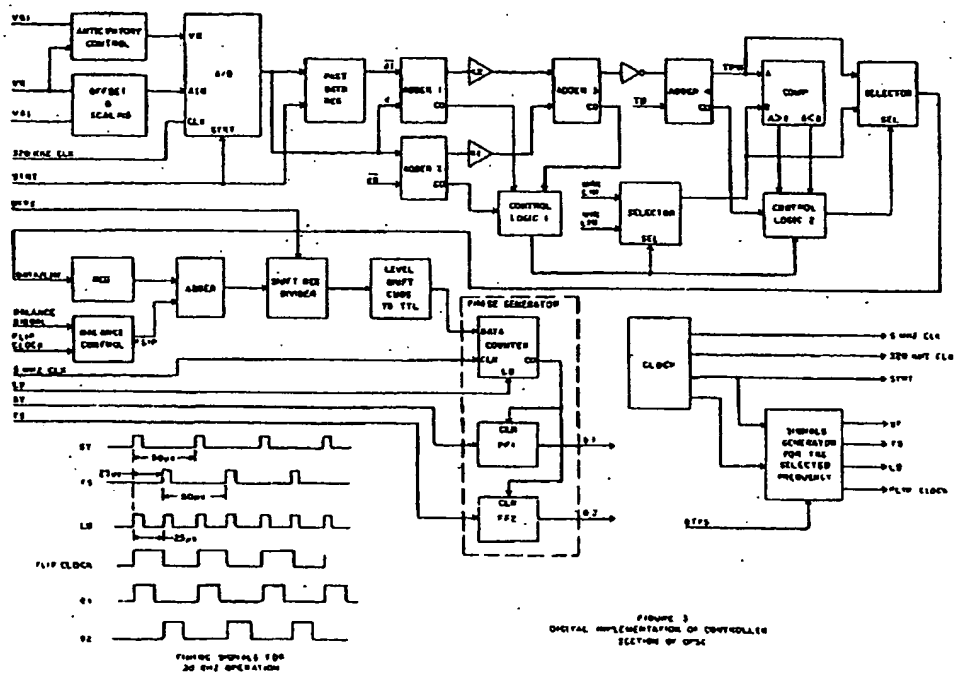
IP1: Voltage level proportional to the current in the primary winding of the transformer.

2.0 FUNCTIONAL DESCRIPTION OF DIGITAL POWER SYSTEM CONTROLLER

To illustrate the overall functionability of the DPSC concept within a typical off-line switching regulator, the reader is referred to the block diagram schematics presented in Figures 1 thru 3. In the Figure 1 diagram, the blocks named "DPSC" and "Signal conditioning network" provide the heart of control of the switching power system. The DPSC block contains all the necessary controls of the sequencing, regulation, system protection, and fault protection diagnostic parameters of the system. The primary function of the signal conditioning network is to provide the necessary interface to the controller through passive scaling elements such that the system can be tailored to specific requirements but still maintain a "universal" DPSC design objective.

2.1 DESCRIPTION OF REGULATION FUNCTION
(Refer to Figures 2 and 3)

For any digital power system controller to function, the primary requirement is to convert the analog signal, which is the output voltage to be regulated, into a digital number for processing to determine the correction needed. This conversion is accomplished by an A/D converter. The digital proportional and derivative feedback control terms are calculated by the digital control processor (DCP). Sum of the feedback control terms (referred to as the correction term) is added to a reference digital quantity corresponding to a nominal pulse width for a given supply. It is further modified by the DCP as a result of balance control signals to correct for the long term imbalance in the inverter transformer.



resulting in a build up of magnetizing current due to unequal volt-sec drive from the switching transistors. This final digital number is translated into duty ratio drive signals Φ 1 and Φ 2 by the phase generator.

The pulse width is set by sampling the regulated output voltage on a periodic basis and the updating of the pulse width through the calculation process. (Note: In the hardware implementation of the DPSC concept, the sampling rate was set at 20 kHz due to A/D and processor cost/performance tradeoffs.)

By monitoring the power supply output voltage, the DPSC can adjust the duty ratio of the drive signals up or down in small discrete steps to counteract the change in the output voltage. The control equation used in this scheme is given as follows. (Refer to Figure 1.)

$$TPW = TA + TCR$$

where TPW = calculated pulse width

TA = nominal pulse width which determines the static output of the given switching power supply

and TCR = pulse width correction

Nominal pulse width, TA, can be calculated by:

$$V_{Anom} \cong V_{Bnom} \times \frac{TA}{T}$$

which gives $$TA = \frac{V_{Anom}}{V_{Bnom}} \times T$$

where V_{Anom} = nominal output

V_{Bnom} = nominal amplitude of voltage at the input of the power filter. (Includes diode and inductor IR losses)

T = switching period

For a 5 V power supply with 12 V input and 40 kHz switching frequency (measured at point B),

nominal pulse width, TA = 5/12 x 25 us = 10.415 us.

With a 5 MHz clock to the phase generator (a counter and a pair of flip flops which converts numbers into duty ratio; refer to phase generator block of Figure 3), this translates into the decimal number 52 for digital processing.

The pulse width correction, TCR, is calculated by: $TCR = -K1(d-d0) - K2(d-d1)$,
where the first term on the right (proportional) feedback control) is to reduce static error and the second term (derivative feedback control) to improve the dynamic response.

d0 = digital equivalent of the nominal output voltage (regulated)

d = digital equivalent of the current (present) sample of the output voltage at A

and d1 = digital equivalent of the preceding sample of the output voltage, VA.

K1 and K2 are digital gain factors. The digital derivative function is approximated by

$$\frac{dVA}{dt} = \frac{(d-d1)}{Ts},$$

where Ts is the sampling period. Ts is absorbed in K2 giving the final form for TCR as shown above.

Changes in the amplitude of the voltage at B are proportional to changes in the amplitude of the power line voltage. Utilization of B, in addition to A, as the duty cycle manipulative information results in an anticipatory or feedforward pulse width modulation scheme resulting in tighter line and load regulation.

How is this accomplished and optimized? Before introducing the analog signal (output voltage) into the A/D converter, it is offset and scaled. The principal relationship between the analog variable and the digital number is proportionality, the repertoire of codes corresponding to a given resolution may represent any portion of the analog voltage or current range. For example, if one wishes to encode the voltage range from 4 to 7 volts in binary, using a 0 - 10 V A/D converter, one could simply apply the voltage without any transformation using only 0.3 of the available number of bits. However, a more efficient alternative would be to offset the input by 4 volts, amplify by 3.33, and apply the resulting 0 - 10 V signal to the converter, thereby making use of the entire range of available codes and improving resolution by a factor of 3. The range of output voltage which is of importance to us is about 4.125 to 5.5 V for a 5 V supply.

2.1.1 Anticipatory Control for Line Regulation

The method of feedforward control is to change the reference voltage VR to the A/D converter according to the line voltage changes, thereby moving the digital codes up or down to counteract the changes in line voltage. Let us review the input/output relationship for the switching power supply:

$$V_A = V_B \times \frac{Ton}{T},$$

where Ton is the ON time and T is the switching period measured at the point, B. This gives

$$Ton = \frac{VA}{VB} \times T$$

with T = 25 us (i.e., fs = 40 kHz) and 5 MHz (0.2 us period) clock to the phase generator, T could be transformed into a decimal number, 25/.02 = 125.

Now we can write our pulse width equation in the form given below considering only the proportional term.

$$\frac{VA}{VB} \times 125 = PWnom - K1(d-d0),$$

where PWnom = nominal pulse width.

$$d = \frac{\frac{VA}{VB} \times 125 - PWnom}{-K1} + d0$$

$$d = \frac{\frac{VAnom}{VBnom} \times 125 - \frac{VA}{VB} \times 125}{K1} + d0$$

Using offset and scaling for the analog input in the form:

$$Ain = 4(VA - 3/4\ VR)$$

where Ain is the offset and scaled analog input and VR is the reference voltage to A/D converter.

$$Ain(nom) = 4(Anom - 3/4\ VRnom)$$

For an A/D with 8 bit resolution, d becomes

$$d = \frac{\frac{VAnom}{VBnom} \times 125 - \frac{VA}{VB} \times 125}{K1} + \frac{4(VAnom - 3/4\ VRnom)}{VRnom} \times 256$$

But

$$d = \frac{4(VA - 3/4\ VR)}{VR} \times 256$$

$$= 1024 \frac{VA}{VR} - 768$$

$$1024 \frac{VA}{VR} - 768 = \frac{\frac{VAnom}{VBnom} \times 125 - \frac{VA}{VB} \times 125}{K1} + \frac{4(VAnom - 3/4\ VRnom)}{VRnom} \times 256$$

For the example case, take

VAnom = 5 V, nominal output voltage

VBnom = 12 V

VRnom = 5.5 V

and K1 = 2

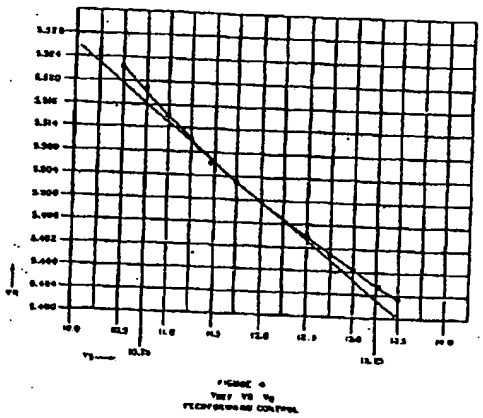
We get

$$\frac{VA}{VR} + 0.061 \frac{VA}{VB} = 0.9346$$

Our aim is to find the relationship between VB and VR which will give a constant output (i.e., VA = 5 V). $VR = \frac{1}{0.1869 - 0.061 \times 1/VB}$

This is the nonlinear relationship between VR and VB and difficult to implement.

Let up plot the curve between VR and VB (Figure 4) to see how it looks in the vicinity of the normal operating point, VR = 5.5 V and VB = 12 V. We will allow +10% variation in the line voltage which is enough for the power supply.



The plotted curve is linear in the range of 11.25 to 12.5 volts of VB and beyond that the nonlinearity increases. Let us consider the range of VB from 10.75 to 13.25 volts.

VB	VR	ΔVR = VRnom ~ VR	ΔVR (AV). Average	ΔVB = VBnom ~ VB
10.75 V	5.5179 V	0.0179 V		
12.0 V	5.5 V	0.012 V	0.01495V	1.25 V
13.25 V	5.488 V			

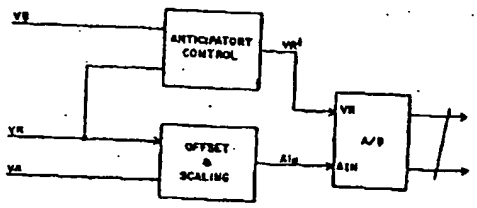
$$\frac{\Delta VB}{\Delta VR} = \frac{1.25}{.01495} = 83.61$$

For normal operating point at VR = 5.5 V and VB = 12 V, the new reference voltage

$$VR' = 5.5 - \frac{\Delta VB}{83.61} = 5.5 - \frac{VB - 12}{83.61}$$

$$VR' = 5.64 - \frac{VB}{83.61}$$

This is the linear equation and can be easily implemented to give the anticipatory control for line regulation. (See below.)



A similar relationship between VA, VB and Ain could be found. Line voltage changes are compensated for by modifying Ain accordingly and keeping the reference voltage VR fixed.

2.2 DESCRIPTION OF BALANCE CONTROL

The use of balance signals is being specified to correct for a long term imbalance in the inverter transformer, resulting in a build up of magnetizing current due to unequal volt-second drive from the power switches.

The effect of balance control operation on magnetizing current (Im) is illustrated in the following figure. A difference of X% in duty cycles of drive signals as a result of balance control operation is introduced, which represents a volt-second imbalance greater than normally expected in the drive electronics. This is done so that the slope of change in magnetizing current, Im, is as independent of the drive electronics as possible. An Im threshold, ±30% of Im (max), is selected which is well below the necessary level of saturation. The DPSC provides a positive and negative threshold detector such that the output is toggled upon the detection of each threshold of opposite sign. When the build up of Im reaches this threshold, the balance comparator (threshold detector) toggles and the DPSC substracts a duty cycle of X/2% from the drive signal which makes the comparator toggle and adds a duty cycle of X/2% to the other drive signal, thus creating a difference of X% in the duty cycle of the drive signals. This forces the Im curve to "walk down", as illustrated in the following figure, until the opposite threshold is reached, where the process is reversed by substracting a duty cycle of X/2% from the drive signal which made the opposite threshold to reach and adds a duty cycle of X/2% to the other drive signal causing a "walk up" and the process is repeated.

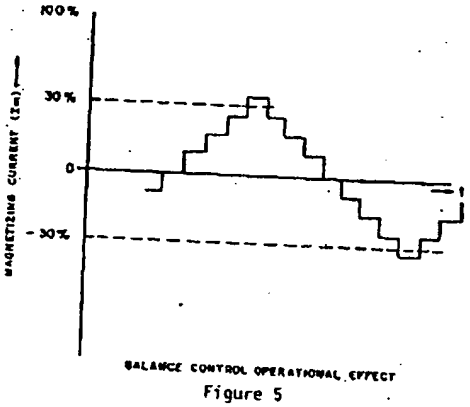


Figure 5

2.3 REGULATION SYSTEM OPERATION - BREADBOARD IMPLEMENTATION

A simplified diagram of the regulator section of the digital power system controller is shown in Figure 3. At the falling edge of the STRT signal to the A/D converter, the analog to digital conversion process starts and is complete in about 30 us (limitation of a MOS ADC). The analog signal is sampled every 50 us. The function of the rest of the circuitry is to (a) calculate $TPW = TA - [k1(d-d0) + K2(d-d1)]$, (b) modify this according to the balance control signals and then, (c) to transform this into duty ratio drive signals $\Phi 1$ and $\Phi 2$. The past data register stores the preceding (past) digital data in the 1's complement form. Adder 1 performs (d-d1) and Adder 2 performs (d-d0), both 2's complement substraction. These terms are multiplied by digital gain factors K1 and K2, respectively. The multiplication becomes easier and simpler, especially when K1 and K2 are integer powers of 2. The operation of shifting a digital number n positions to the

left corresponds to multiplying it by 2^n. Shifting a digital number n positions to the right corresponds to multiplying it by 2^{-n}. This could be achieved by using shift registers performing shift operations as desired or through hard wire strappings. The Adder 3 sums these terms together producing K1(d-d0) + K2(d-d1). This sum could be positive or negative. It is in 2's complement form if negative and in true data form if positive. Adder 4 performs the operation TA + [-T3] giving TPW. Where TA is the hard wired digital number corresponding to nominal pulse width for the given supply. According to the sign of [-T3], the control logic 1 selects the maximum or minimum limit which is set to 9% and 41% duty ratio. This is compared with TPW. Control logic 2 selects the TPW data or appropriate limit as a result of comparison. If the TPW data is greater than the maximum limit, then the maximum limit is selected. If it is less than the minimum limit, then the minimum limit is selected. Otherwise, the TPW data is selected. This data or limit is stored in a register. This data is further modified by the balance control signal and the flip clock. It adds 4% of duty ratio to data corresponding to one phase and substracts 4% from the other phase (Φ 1 and Φ 2) or vice versa, depending on the state of flip signal. The counter and flip flops convert this final digital number into a duty ratio (drive signals Φ 1 and Φ 2).

2.4 DIAGNOSTICS AND SYSTEM PROTECTION PHILOSOPHY

Present analog methods and power system architectures do not lend themselves to elaborate protection schemes and self-diagnostics to a submodule level. A higher maintenance, repair and component costs are due to system complexity of analog systems. As a result of the present digital approach, there is savings in maintenance/repair and assembly costs due to integrated diagnostic functions. The encoded fault at the subassembly level is stored in a fault register for use by the serviceman. The fault is displayed (LED) for a short period of time (about 15-20 seconds) on command to facilitate the easy replacement of the damaged parts. It requires only 5 bits of memory to store as many as 31 faults and requires a 5 LED display.

2.4.1 Fault Diagnostics

The reader is referred to Figures 1 and 2 to understand the operation of the fault diagnostics. Two important signals, VB and I, are utilized in the fault determination scheme. Although VB and I signals are oscillatory, only their peak values are of interest. The strobe generating circuit of the DPSC generates strobes at the middle of the on time of drive signals (Φ 1 and Φ 2). The DPSC strobes (monitors) VA1, VB1, I1 and Ip inputs giving them sufficient time to settle down before being strobed. It checks for specific combination of conditions to occur for a prescribed number of times successively to determine the catastrophic failure of certain elements in the power system. Some of the failure modes are monitored during the "power up sequence" and "regulation mode" while others during the later only. The fault conditions are the combination of voltage and current levels on these inputs. Elements in the power filter stage, such as diodes, inductor and capacitor are checked for failure modes as open or short. The faults are priority encoded to avoid chain reaction catastrophic failures. Highest priority is given to the most destructive fault. The detected and encoded fault condition is stored and displayed (LED's) on command providing easy serviceability.

For example, one such condition for fault recognition for shorted diodes (D1 and D2) could be:

FDS = (I1VH. VB1L.STB)FC1,

where I.VH indicates current level on I1 input very high, greater than the certain percent of its normal peak value. VB1L is the voltage level corresponding to the voltage at point B, being less than a preset percent of its normal value. STB is the appropriate strobe signal and FC1 is the number of successive times the condition should hold (in this case 1).

2.4.2 System Protection

The description of system protection functions is as follows:

(i) Output Over Voltage: When the voltage level at point A rises above the predetermined threshold value and stays there for a certain period of time to avoid nuisance tripping, the over voltage fault is detected, encoded and stored. This fault condition is displayed (LED) and switching inhibited. This condition is not strobed but continuously monitored.

(ii) Secondary Circuit Over Current: When the inductor current rises above the predetermined current level, the DPSC outputs (forces) the minimum pulse width so long as that condition exists and then goes to a normal operating mode.

(iii) Primary Overcurrent: When the detected current, Ip, at the primary side of the transformer rises above the predetermined threshold, the fault is detected, encoded and stored. The fault condition is displayed (LED) and switching signals (drive signals) are inhibited. This signal is continuously monitored and not strobed because of the severity of its effects and damages.

3.0 RESULTS

An actual breadboard prototype using CMOS/TTL logic was constructed and various tests were performed on a 5 V, 12 A, double ended, half bridge power supply. Although the breadboard contained diagnostic and system protection functions, only the regulation performance is described here. The following is an example of the regulation performance. Refer to Figure 5.

	Dynamic Load Change	
	12A to 6 A	6A to 12 A
Initial Excursion =	500 mV	50 mV
Recovery Time =	800 us	600 us
Static Error =	~0	~0

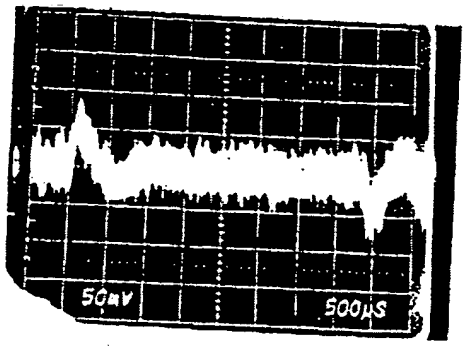


Figure 6 - Dynamic Load Effect

Results of with and without the anticipatory control are depicted below for line changes from 104 VAC to 127 VAC for minimum (20%) and maximum (100%) load conditions.

(i) Without compensation control

AC Line Voltage	Output Voltage VA With Min. Load 2.4 A	Max. Load 12 A
104 VAC	5.047 V	5.032 V
115 VAC	5.065 V	5.049 V
127 VAC	5.081 V	5.066 V
Change in output voltage	Δ VA = 34 mV	Δ VA = 34 mV

Total load/line regulation:
VA = 49 mV (~ 1%)

(ii) With compensation (control)

AC Line Voltage	Output Voltage VA With Min. Load 2.4 A	Max. Load 12 A
104 VAC 115 VAC 127 VAC	5.017 V 5.018 V 5.016 V	5.008 V 5.006 V 5.004 V
Change in output voltage	VA = 1 mA	δVA = 4 mV

Total load/line regulation:
VA = 14 mV ($\sim$ 0.3%)

4.0 CONCLUSION

Using microcontroller system feedback and control, an optimal, versatile digital power system controller with features outlined can be developed into a single LSI chip. The results of the breadboard evaluation has identified that excellent line and load regulation which competes with present analog systems can be accomplished. Through programmability, it offers flexibility and adaptabilility to different designs. The fault diagnostic features is the "kohinoor" of the crown not found in the analog systems. It offers easy serviceability and maintainability of the power systems. A multilevel power supply could be regulated using the same controller by multiplexing the outputs.

As of the writing of this paper, NCR is entering into a custom LSI design phase of the OPSC concept. The LSI chip, which contains all the sequencing, regulation, system protection, and fault isolation diagnostic functions, as described, is being implemented in NMOS technology to support up to a triple output power system.